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Submicron Single-Gate and Dual-Gate GaAs MESFET's with Improved Low Noise and High Gain Performance

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Abstract—**Microwave performance of single-gate and dual-gate GaAs MESFET's with submicron gate structure is described. Design consideration and device technologies are also discussed. The performance of these GaAs MESFET's exceeds previous performance with regard to lower noise and higher gain up to *X* band: 2.9-dB noise figure (NF) and 10.0-dB associated gain at 12 GHz for a 0.5-μm single-gate MESFET, and 3.9-dB NF and 13.2-dB associated gain at the same frequency for a dual-gate MESFET with two 1-μm gates.**

I. Introduction

SINGLE-GATE [1], [2] and dual-gate [3], [4] GaAs MESFET's have been extensively developed, showing low noise and high gain properties at microwave frequencies. Improvements have been successfully attained mainly due to gate length reduction. As a result of advanced photolithography 0.5-μm-gate MESFET's with 4–5-dB noise figures (NF) at 12 GHz have been realized [2].

However, calculations on the NF [5] revealed that the observed NF values were still large compared with the theoretical ones. The discrepancy is considered to be partly due to the degraded crystal quality in the epitaxial film near the substrate and partly due to the effects of parasitic resistances. This suggests that refinement of epitaxial growth and metallization technologies is more urgently required than further gate length reduction to produce decreased NF.

The purpose of this work is to realize improved GaAs MESFET's based on refinement of these technologies. Details of epitaxial wafer preparation and of contact metallization processes are described in Section II. Design consideration and fabrication of single-gate (0.5-μm-gate and 1.0-μm-gate) and dual-gate (1-μm–1-μm-gate) MESFET's are described in Section III. MESFET microwave performance is described in Section IV.

Manuscript received September 26, 1975; revised December 18, 1975.
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II. Device Technology Refinement

A. Epitaxial Wafer Preparation

The gallium arsenide wafer used in this work consists of a thin and highly doped n-type active layer, a high-resistivity buffer layer, and a semi-insulating substrate. Both buffer and active layers were successively grown on the substrate in the modified $Ga/AsCl_3/H_2$ reaction system [6].

1) Buffer Layer: At the dc bias point, where minimum NF is observed, carriers are confined in an approximately 100-Å-wide n-type epitaxial region adjacent to the substrate. Thus crystal properties, such as electron mobility and impurity concentration in this region, have the dominant effect on MESFET performance.

Electron mobility degradation in the region near the

substrate is often observed when the n-type active layer is epitaxially grown directly on the Cr-doped semi-insulating substrate. This degradation appears to be due to crystal defects and/or to deep-level impurities (Cr) which diffused out of the substrate. It was found that mobility degradation could be eliminated in a wafer on which an active layer was successively grown on an epitaxial buffer layer [6]. The high resistivity property ($n \simeq 10^{13}$ cm^{-3}) of the buffer layer was obtained by preventing the doping with donor impurities by means of an additional bypass $AsCl_3/H_2$ flow in the epitaxial process. The distribution of electron Hall mobility in the epitaxial layers was estimated by Hall measurement, using a Hall element which had a Schottky contact on its surface [6]. Two wafers, one with a buffer layer and one without a buffer layer, were used. The n-type active layer doping level of two wafers was 7×10^{16} cm^{-3}. Results are shown in Fig. 1. The electron mobility gradually decreased towards the interface for a wafer without a buffer layer. For a wafer with a buffer layer, electron mobility gradually increased to the value of the buffer layer. Buffer layer Hall mobility (6000 $cm^2V^{-1}s^{-1}$) was found to be low, as compared with the mobility of a high purity layer (7000–8000 $cm^2V^{-1}s^{-1}$ for a doping level of about 10^{13} cm^{-3}). The reason may be that the buffer layer was compensated in some degree.

2) n-type Active Layer with High Doping Level: Drangeid and Sommerhalder [7] have predicted that the microwave performance of MESFET's would be improved by increasing the carrier concentration in the channel. This was qualitatively confirmed by the present experiment, as shown in Fig. 2. Fig. 2 shows the NF and the associated power gain at 8 GHz versus carrier concentration measured for the present 0.5-μm-gate MESFET's. These results clearly suggest that the doping level in the channel should be increased until the gate breakdown voltage sets an upper limit.

The Schottky-contact breakdown voltage is said to be inversely proportional to the doping level and is about -10 V for 1×10^{17} cm^{-3} in the case of n-GaAs [8]. However, this seems not to be the case in an actual MESFET in which the active layer is extremely thin (≤ 0.2 μm). The breakdown voltage was found to depend more strongly on the separation between the gate and the adjacent ohmic contacts than on the doping level. As shown in Fig. 3, a breakdown voltage higher than -10 V can be ensured even at the doping level of 2.5×10^{17} cm^{-3}, provided that the separation between the contacts has been chosen larger than 0.6 μm. In the present device fabrication, the doping level in the active layer was thus chosen around 2.5×10^{17} cm^{-3}.

B. Metallization Technology

The MESFET noise performance is sensitively affected by parasitic resistances, such as source series-resistance R_s and gate-metallization resistance R_g. The minimum NF was calculated at 12 GHz as a function of the total parasitic resistance, $R_s + R_g$, based on Statz's model [5] for a MESFET with 0.5-μm gate length, 280-μm gate width, and 2.5×10^{17}-cm^{-3} carrier concentration in the channel. The

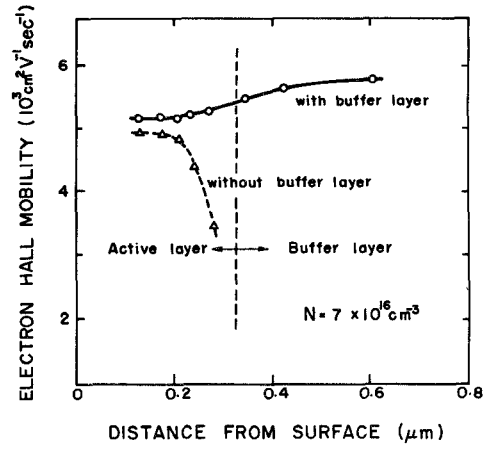

Fig. 1. Electron Hall mobility distribution in two wafers, with a buffer layer (solid line) and without a buffer layer (broken line). Vertical line indicates active layer interface.

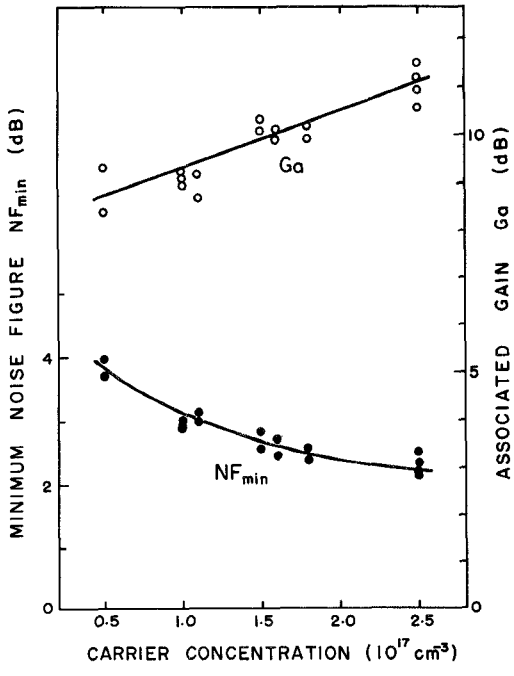

Fig. 2. Minimum NF and associated gain at 8 GHz versus carrier concentration in an n-type active layer measured for 0.5-μm single-gate MESFET's. Bias condition: $V_D = 2.0$ V, $I_D = 10$ mA.

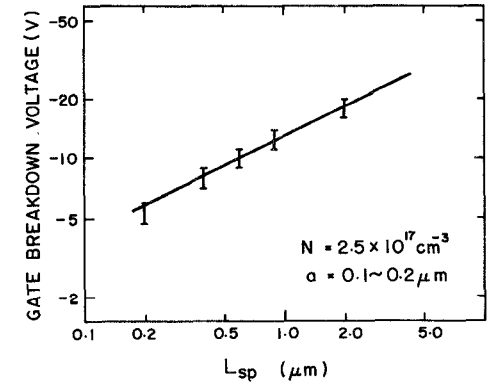

Fig. 3. Gate breakdown voltage V_B versus spacing L_{sp} between Schottky-gate and ohmic contacts (V_B is defined as the reverse voltage at which a gate leakage current of 10 μA flows).

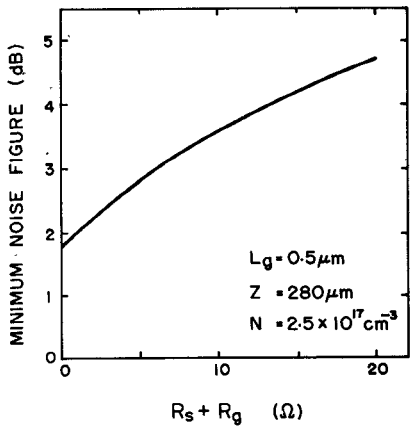

Fig. 4. Calculated minimum NF at 12 GHz versus total parasitic resistance, $R_s + R_g$.

result shown in Fig. 4 predicts that $R_s + R_g$ should be reduced below 5 Ω in order to obtain a NF less than 3 dB at 12 GHz.

1) Gate-Metallization Resistance: Aluminum is preferred as a gate metal because it has a low resistivity and satisfactory characteristics as a Schottky contact to n-GaAs. Reproducible fabrication of a gate pattern that consists of an aluminum film thicker than the gate length would be difficult. Thus a gate structure having more than one gate pad becomes desirable to reduce the gate-metallization resistance in the case of a submicron gate structure.

2) Source Series-Resistance: In order to reduce the source series-resistance, it is necessary to use a technique that produces ohmic contacts with low specific contact resistance. It is well known that the quality of the contacts is strongly influenced by wafer surface cleaning before evaporation. Wafers used in the present work were thoroughly rinsed in organic solvents (trichloroethylene and acetone) and then lightly etched in warm phosphoric acid. This chemical etching was effective in removing native oxides on the wafer surface. The ohmic contacts used in the present device were made by alloying a gold–germanium evaporated film with eutectic composition, covered with a Ni film at 450°C in a hydrogen atmosphere. The Ni-film thickness was optimized to minimize specific contact resistance degradation during high temperature storage.

Three wafers were prepared to measure specific contact resistance: a nondoped boat-grown wafer with $n = 2 \times 10^{16}$ cm^{-3} and two kinds of epitaxially grown wafers having a thin n-type layer ($n = 7 \times 10^{16}$ cm^{-3} and 1.6×10^{17} cm^{-3}, respectively) on a Cr-doped substrate. The specific contact resistance of the contact on the boat-grown wafer was calculated from data measured on the test structure described by Cox and Strack using curve-fitting techniques [9]. Specific contact resistance of contacts on epitaxially grown wafers was measured by the transmission line model (TLM) method [10]. The improved specific contact resistance in the present work is shown in Fig. 5, as compared to that reported in [11].

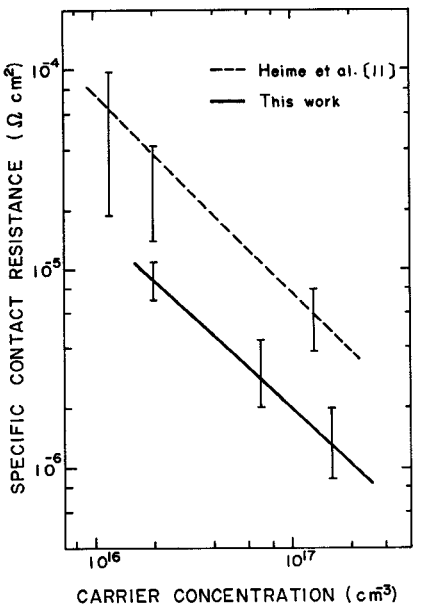

Fig. 5. Specific contact resistance variation with differing doping level in n-GaAs.

Electron probe microanalysis has also shown that the present ohmic contact system is metallurgically and electrically stable during elevated temperature (330°C) storage [12].

III. Device Description

Three types of GaAs MESFET's were fabricated: 0.5-μm single gate, 1-μm single gate, and 1-μm–1-μm dual gate. Dimensions of these MESFET's are shown in Table I. Fig. 6(a)–(c) show top views of these devices. Fig. 7 shows a SEM view of the 0.5-μm-gate pattern.

In the GaAs wafers used for the fabrication, a 5-μm-thick buffer layer with a carrier concentration of 1×10^{13} cm^{-3} was sandwiched between the active layer and the Cr-doped semi-insulating substrate. The carrier concentration and the thickness of the active layer were 2.5×10^{17} cm^{-3} and 0.15 μm, respectively.

Gates were formed using 0.5-μm-thick aluminum-film stripes patterned reproducibly by optical lithography using a chromium mask. For the 0.5-μm-gate device, a dual-gate-pad structure was adopted to get a low gate-metallization resistance. The gate-metallization resistance which contributes to the input loss has been estimated as $\frac{1}{3}$ of the metallization resistance, measured from one end to the other of the gate [13]. Thus, in all types of the present MESFET's, gate-metallization resistance was expected to be reduced to less than 1 Ω.

Source and drain ohmic contacts were formed by alloying a 0.15-μm-thick gold–germanium film covered with a thin Ni film. The spreading resistance at the source contact was estimated as low as 1 Ω as measured by the TLM method, using 1×10^{-6} Ω·cm as the value of the specific contact resistance. The resistance corresponding to the epitaxial layer resistance between source and gate was calculated

TABLE I
DIMENSIONS OF THREE MESFET'S

Device	Gate Length (μm) G_1	G_2	Electrode Separation (μm) S-G_1	G_1-G_2	S-D	Gate Width (μm)
0.5μm single-gate	0.5	—	0.8	—	2.3	280
1μm single-gate	1.0	—	1.0	—	3.0	300
dual-gate	1.0	1.0	1.0	3.0	7.0	300

S: Source D: Drain G_1: First-gate G_2: Second-gate

TABLE II
TYPICAL DC CHARACTERISTICS OF THREE MESFET'S

Device	Gate Pinch-off Voltage (V)	Transconductance (mmho)	Gate Breakdown Voltage (V)
0.5μm single-gate	−2.0	24 (V_D = 2.0V, I_D = 10 mA)	−13 (I_G=−10μA)
1μm single-gate	−2.0	24 (V_D = 2.0V, I_D = 10mA)	−15 (I_G=−10μA)
dual-gate	−3.0	21 (V_D= 4.0V, V_{G2}= 0V, I_D= 10mA)	−15 (I_G=−10μA)

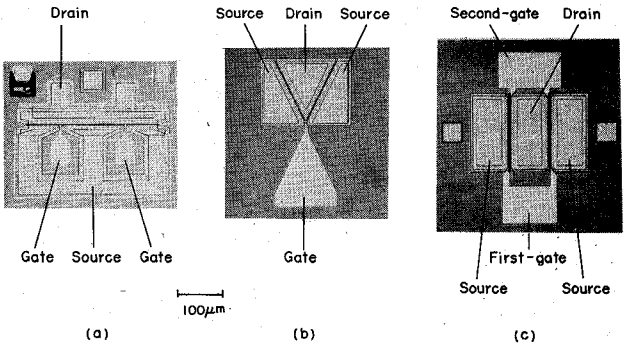

Fig. 6. Top views of three types of MESFET's. (a) 0.5-μm single-gate. (b) 1-μm single-gate. (c) 1-μm–1-μm dual-gate.

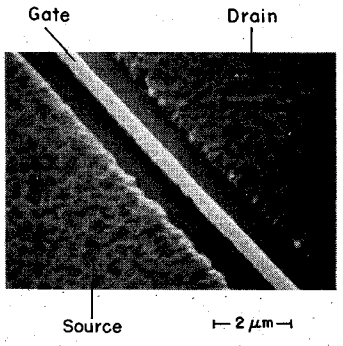

Fig. 7. 0.5-μm-gate MESFET SEM view.

as approximately 2 Ω. Consequently, the source series-resistance could be reduced to less than 3 Ω. Additional Au films were deposited on the source and drain contacts to make wire bonding easy.

Single-gate and dual-gate MESFET dc characteristics are summarized in Table II. The *I–V* characteristics of the 0.5-μm-gate MESFET are shown in Fig. 8. The improved characteristics, i.e., absence of looping in the drain current, and the high transconductance[1] at low drain current may be due to the elimination of the crystal defects and/or the deep level impurities near the interface with the buffer layer. Both low saturation-voltage and high transconductance indicate that source series resistance is satisfactorily reduced.

[1] This high transconductance has not been measured for a wafer prepared by vapor-phase epitaxial growth technique.

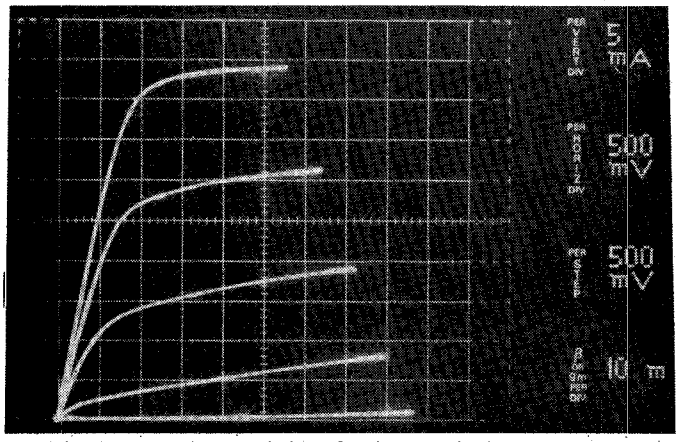

Fig. 8. *I–V* characteristics of a 0.5-μm single-gate MESFET.

Aging tests of the present MESFET's at an elevated temperature were also performed. The estimated MTF at the operating temperature exceeds 10^8 h [14].

IV. Noise Figure and Power Gain at Microwave Frequencies

NF's and power gains of single-gate and dual-gate MESFET's were directly measured in the frequency range from 4 to 12 GHz, using a precision automatic noise figure indicator (Ailtech Type 75) and a network analyzer (HP 8410A). The drain and gate pads of these MESFET's were bonded into 50-Ω striplines. The bias voltages were chosen to give the lowest NF: I_D = 10 mA, V_D = 2 V for single-gate, and I_D = 10 mA, V_D = 4 V for dual-gate MESFET's. Results, measured under conditions of minimum noise and maximum gain at 4, 8, and 12 GHz, are summarized in Table III. Frequency dependences of minimum NF and associated power gain are also shown in Fig. 9.

For the 0.5-μm-gate MESFET, a maximum frequency of oscillation above 90 GHz was extrapolated from unilateral gain, calculated from measured *s*-parameters in the 2–16-GHz frequency range.

Wide gain-control capability of dual-gate MESFET is shown in Fig. 10. More than 11-dB gain suppression is possible at 8 GHz with less than 5-dB NF degradation.

Gain and NF performance of MESFET's described in this paper are the most advanced reported to date.

TABLE III
POWER GAIN G AND NF MEASURED UNDER MINIMUM NOISE AND MAXIMUM GAIN CONDITIONS

Device \ Frequency		4 GHz		8 GHz		12 GHz	
		G(dB)	NF(dB)	G(dB)	NF(dB)	G(dB)	NF(dB)
0.5μm single-gate	G Max.	18.9	1.6	13.8	2.7	12.3	4.3
	NF Min.	15.2	1.1	11.2	2.2	10.0	2.9
dual-gate	G Max.	20.6	2.4	14.9	4.2	13.5	5.0
	NF Min.	19.6	1.4	14.1	3.2	13.2	3.9

Note: Bias condition: $V_D = 2.0$ V, $I_D = 10$ mA for a single-gate MESFET and $V_D = 4.0$ V, $V_{G2} = 0$ V, $I_D = 10$ mA for a dual-gate MESFET.

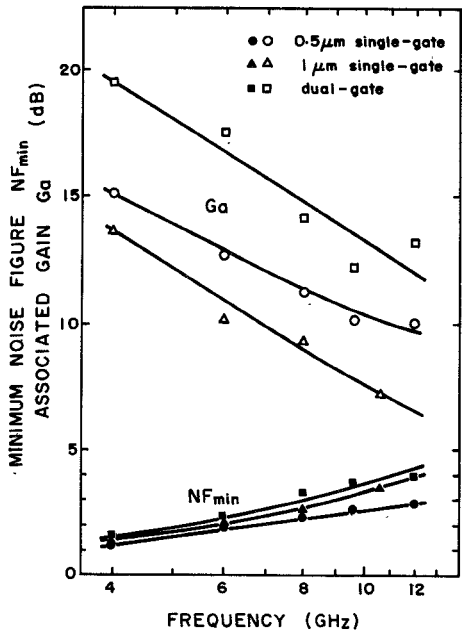

Fig. 9. Frequency dependence of minimum NF and associated gain for the three types of MESFET's. Bias condition: $V_D = 2.0$ V, $I_D = 10$ mA for single-gate MESFET's, and $V_D = 4.0$ V, $V_{G2} = 0$ V, $I_D = 10$ mA for a dual-gate MESFET.

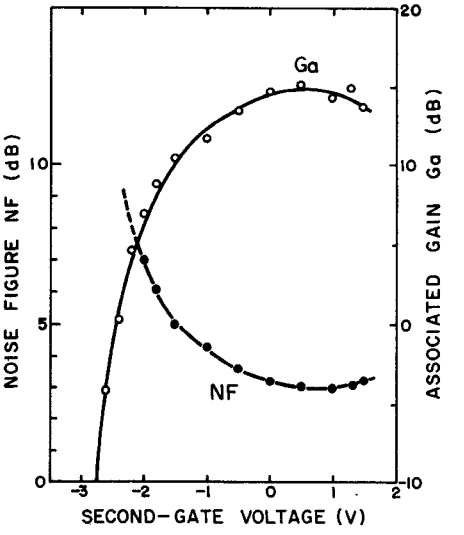

Fig. 10. NF and associated gain versus second-gate voltage for a dual-gate MESFET measured at 8 GHz. Bias condition: $V_D = 4.0$ V, $V_{G1} = -2.2$ V. External circuit impedances were chosen to minimize the NF at $V_{G2} = 0$ V.

V. CONCLUSION

Submicron single-gate and one-micron dual-gate MESFET's have been fabricated, based on design considerations and on refined fabrication techniques, including those of epitaxial growth for high crystal quality and of metallization for low parasitic resistances.

Microwave measurements of these MESFET's were carried out at frequencies up to 12 GHz. The performance values obtained are the best reported to date with respect to lower NF and higher gain: 2.9-dB NF and 10.0-dB associated gain at 12 GHz for the 0.5-μm single-gate MESFET's and 3.9-dB NF and 13.2-dB associated gain at the same frequency for the dual-gate MESFET's. The high reliability of the present MESFET's (expected MTF $\geq 10^8$ h) is being improved.

ACKNOWLEDGMENT

The authors would like to express their appreciation to Dr. S. Asanabe and Dr. T. Irie for their useful discussions and warm encouragement. They also thank M. Ishikawa for his advice in device fabrication, Dr. H. Terao and K. Noguchi for providing the GaAs epitaxial wafers, and I. Nagasako for his advice in microwave measurements.

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A Power Silicon Microwave MOS Transistor

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Abstract—**Vertical MOS silicon power transistors for microwave power applications have been fabricated using an angle evaporation technique to position the gate electrode on the side of a mesa. These devices have produced 3-W output power at 1.5 GHz as a Class *B* amplifier and exhibit excellent linearity and noise properties. Device modeling has shown that parasitic capacitances are the chief factor limiting the frequency response, and the prospects for useful devices at 4 GHz are good.**

I. Introduction

THE frequency of operation of silicon MOS transistors has been extended to microwave frequencies in the past few years through the use of fairly sophisticated ion-implantation [1] and diffusion [2], [3] technologies. With these technologies, gate lengths on the order of 1 μm were achieved in small-signal transistor devices which demonstrated useful power gains in the 1–4-GHz frequency range. The extension of the implantation and diffusion (D-MOST) technologies to the development of large gate periphery, short channel devices for microwave power applications has not been reported to date.

Recently, a third technology (VMOST) was reported [4] which promised the processing of large periphery microwave MOST devices with high yield. Class *A* output power levels of up to 1.5 W at 0.7 GHz were obtained from a transistor cell having a total gate periphery of 0.62 cm. The VMOST structure has a mesa-type geometry, as shown in Fig. 1, which is formed by isotropic chemical etching.

Manuscript received October 13, 1975; revised December 13, 1975. This work was supported in part by the Office of Naval Research, Washington, DC, under Contract N00014-74-C-0012.

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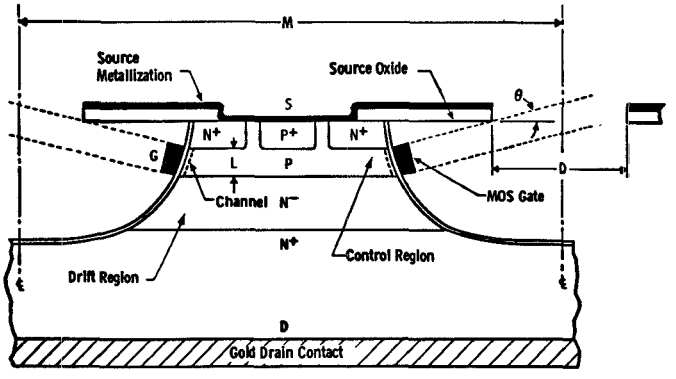

Fig. 1. Topology of vertical power MOS transistor geometry.

The length of the vertical n-channels is controlled by epitaxial growth, and the metal gate length by an angular metal deposition. This technology, referred to from now onwards as the ©VMOST technology, is distinctly different from the *V*-groove process [5] which uses a hydrazine anisotropic etch to form *V*-grooves. The gate in the *V*-groove transistor completely covers the oxidized etched surface, thereby giving rise to excess parasitic gate-drain capacitance which is detrimental to high frequency performance.

This paper will attempt to bring up to date progress which has been made in improving the power and frequency performance of the VMOST device. Descriptions of the latest device design and fabrication procedures are given in the next two sections. The microwave performance of some typical devices is shown in Section IV, while in Section V computer modeling results of the transistor are presented.